

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

Fig. 2

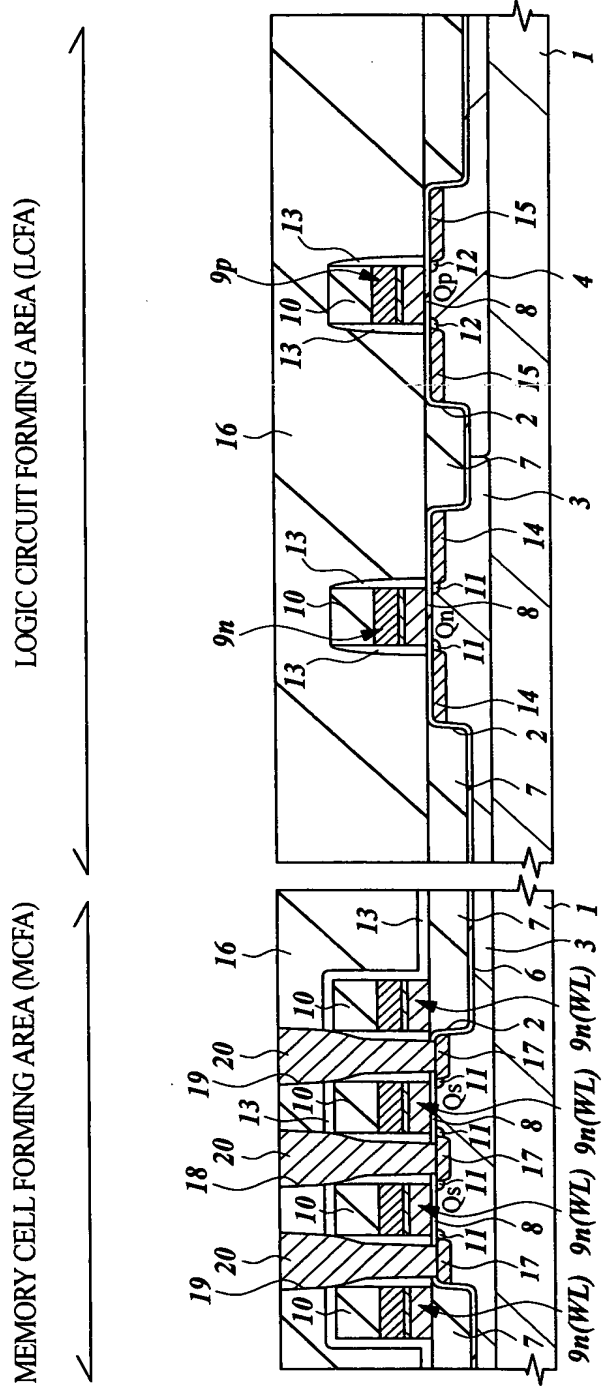


Fig. 3

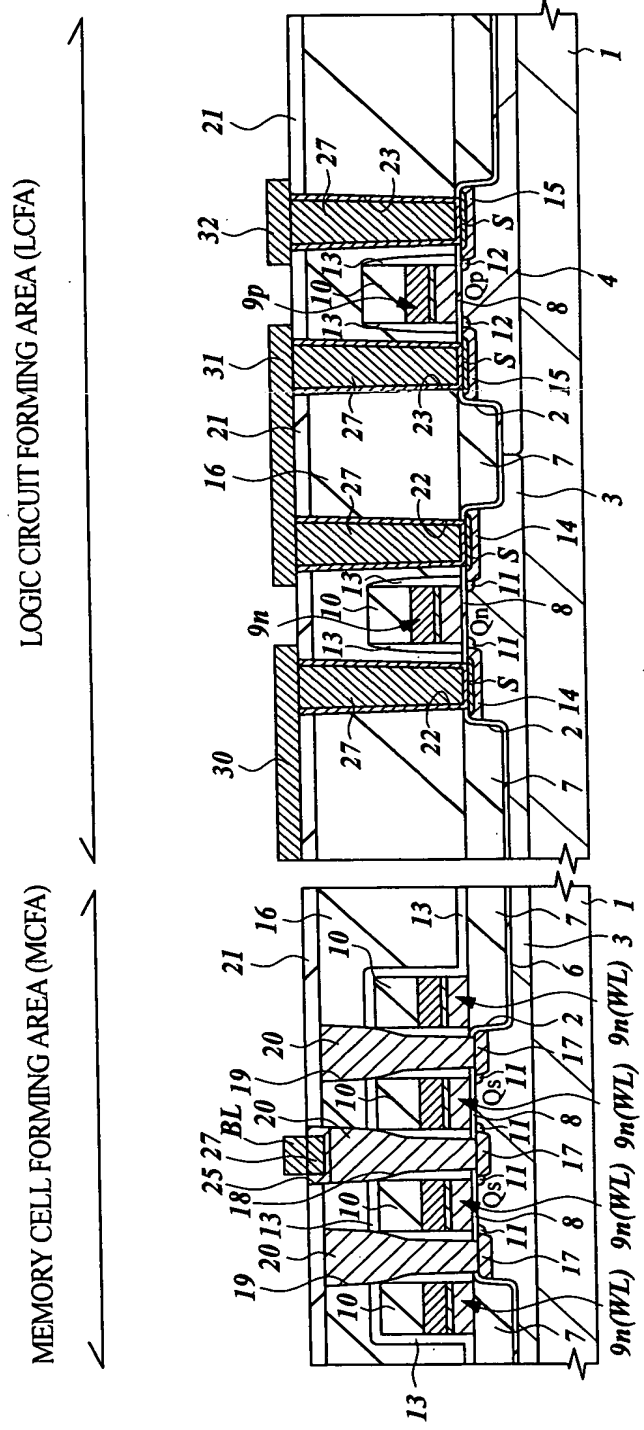


Fig. 4

MEMORY CELL FORMING AREA (MCFA)

LOGIC CIRCUIT FORMING AREA (LCFA)

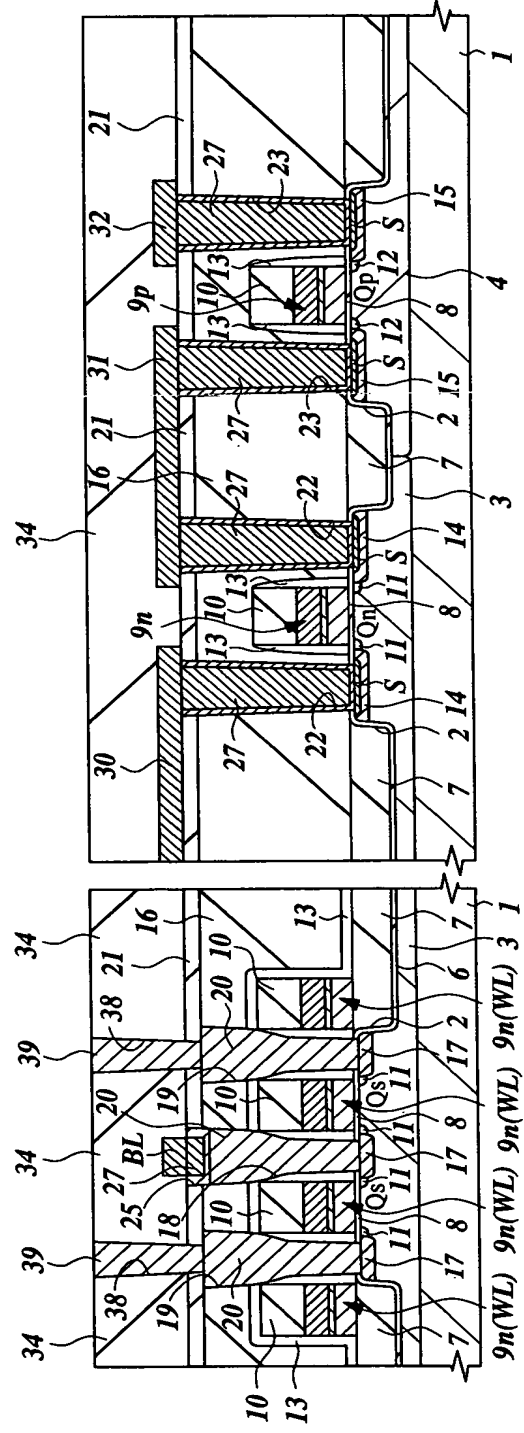


Fig. 5

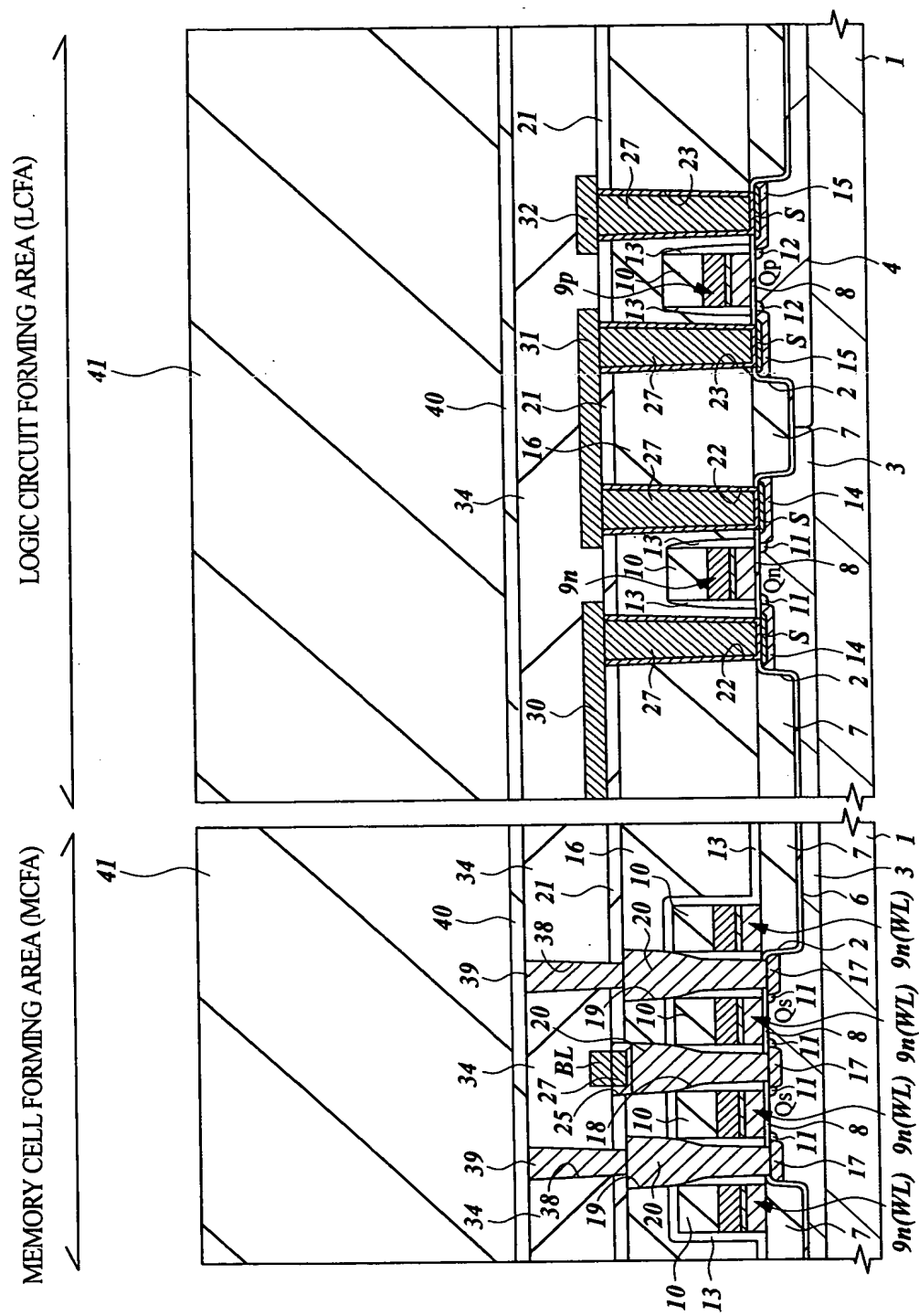


Fig. 6

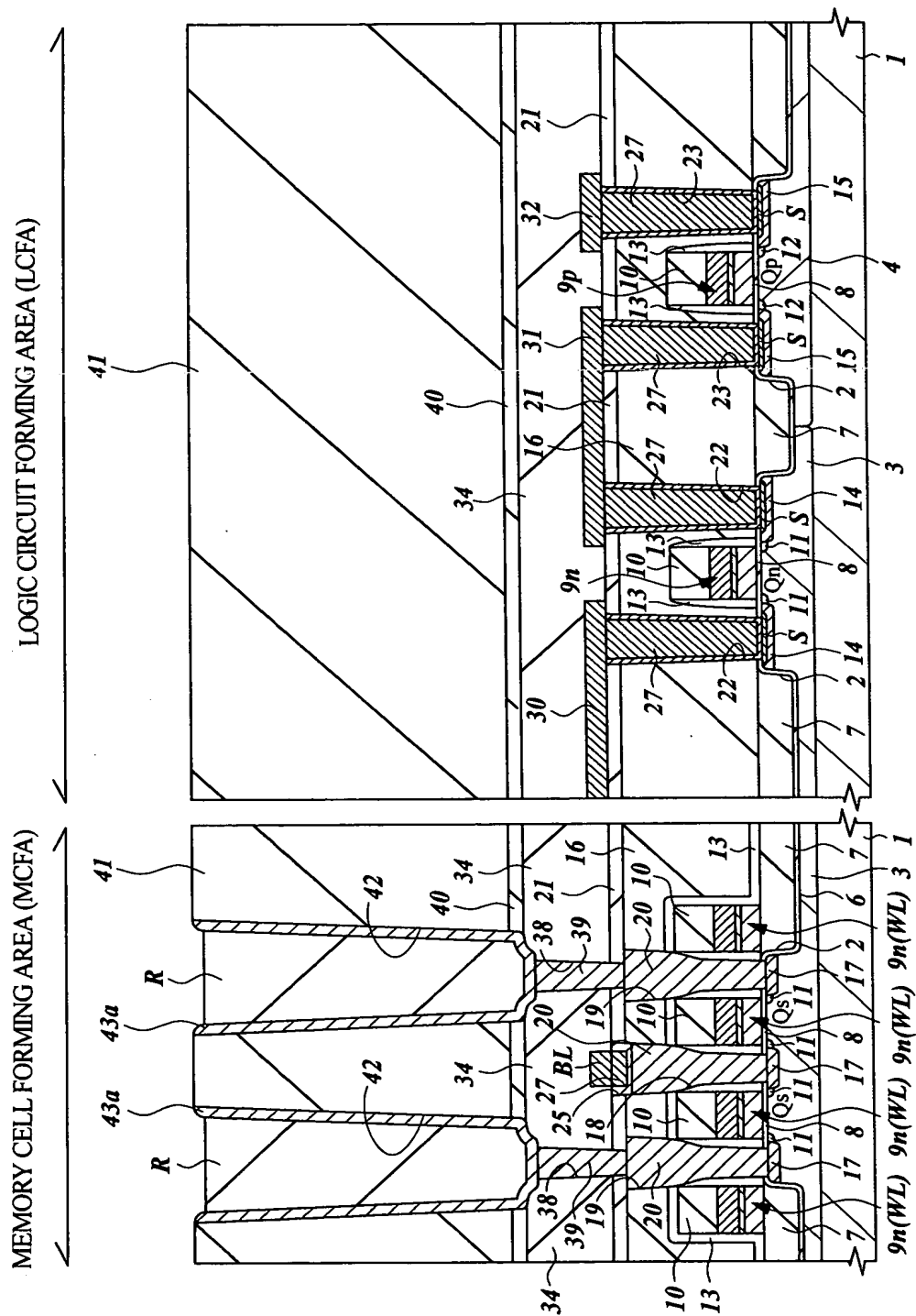


Fig. 7

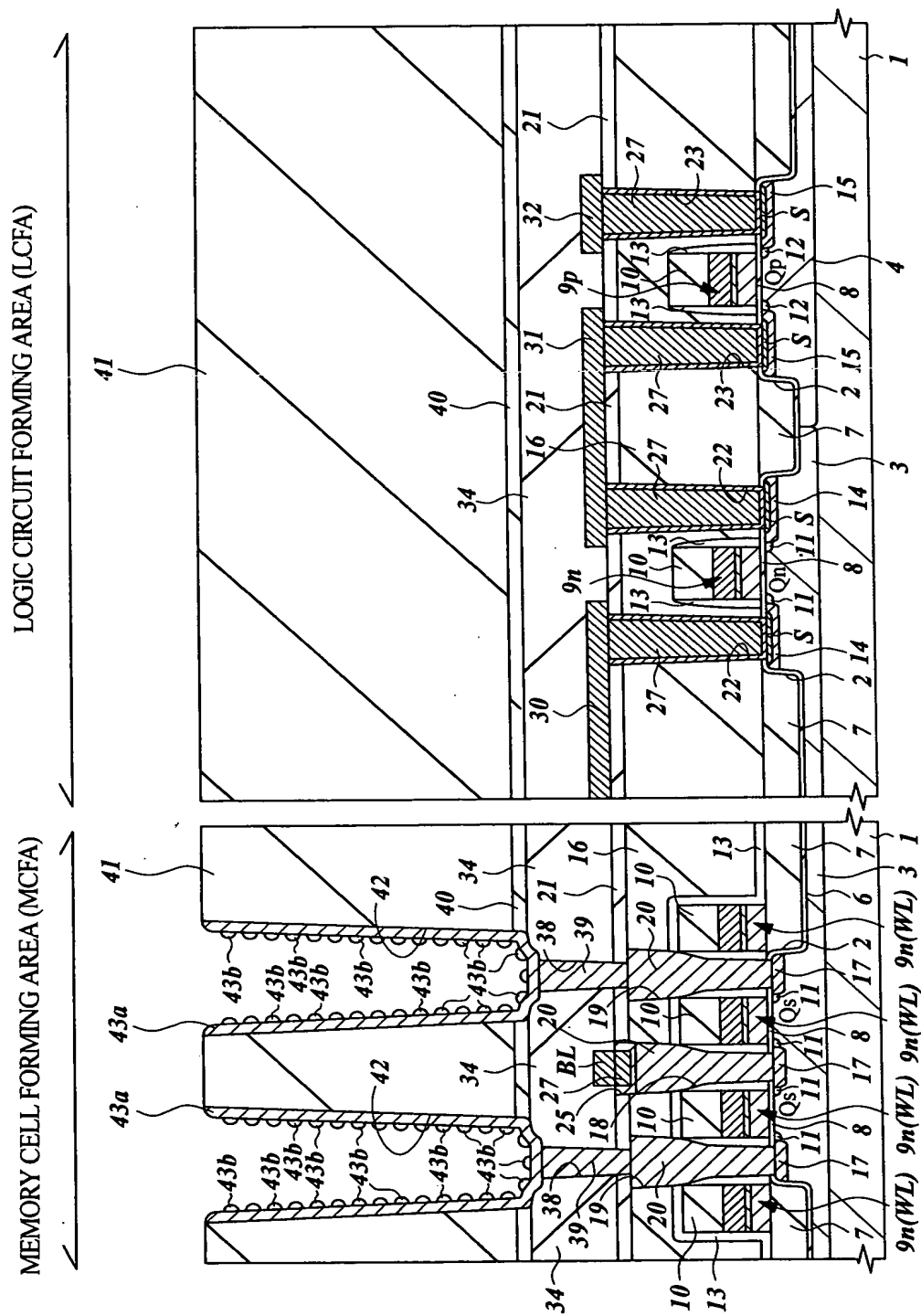


Fig. 8

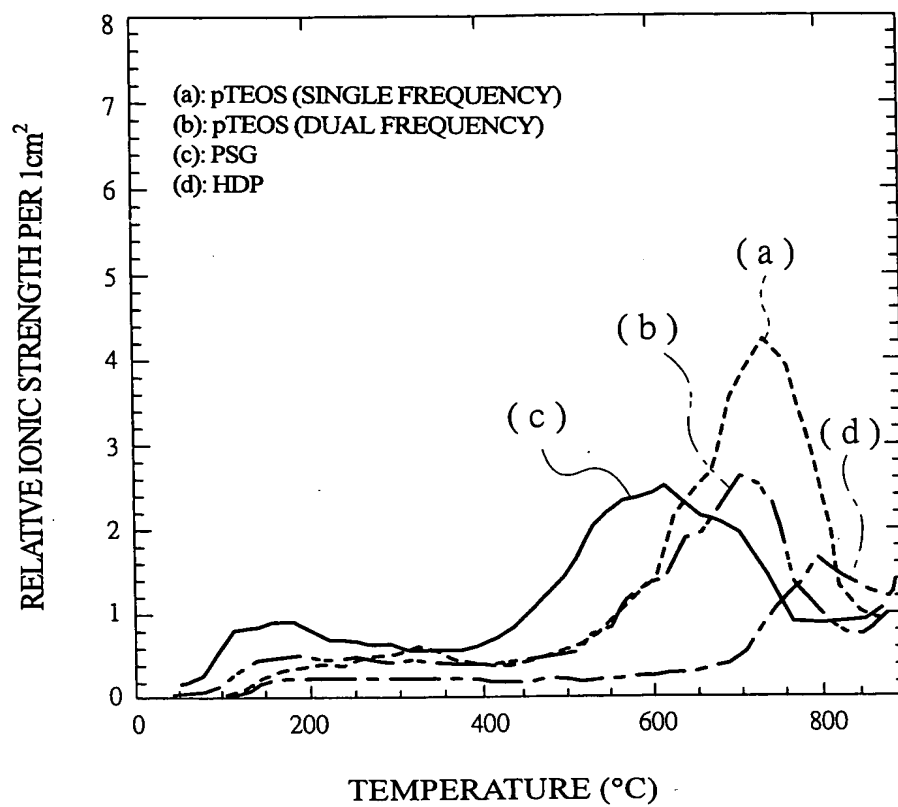


Fig. 9

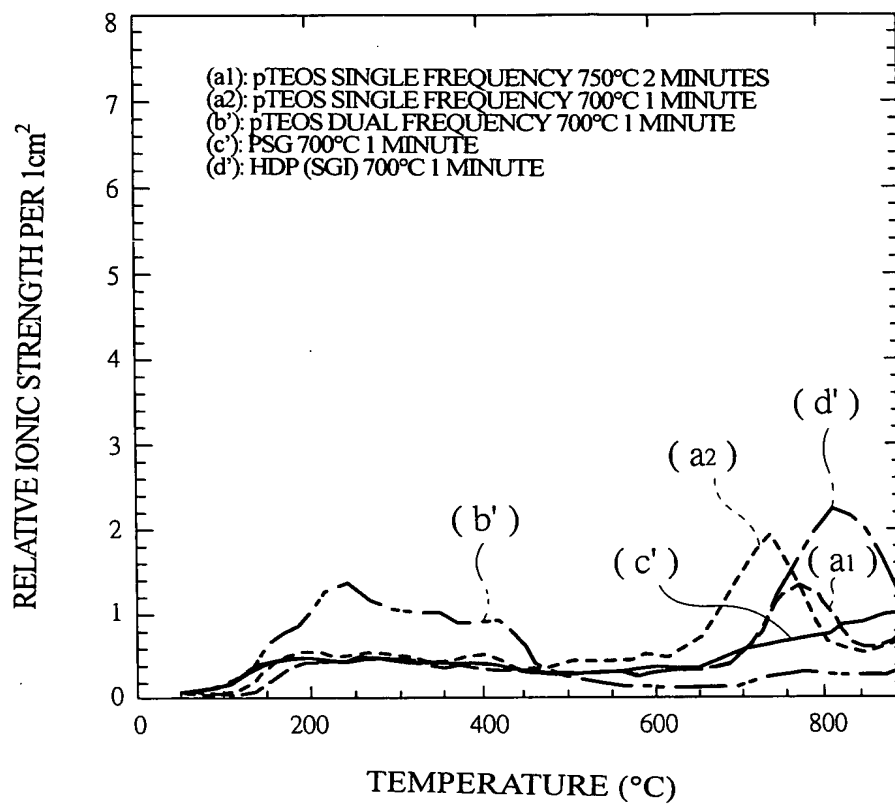


Fig. 10

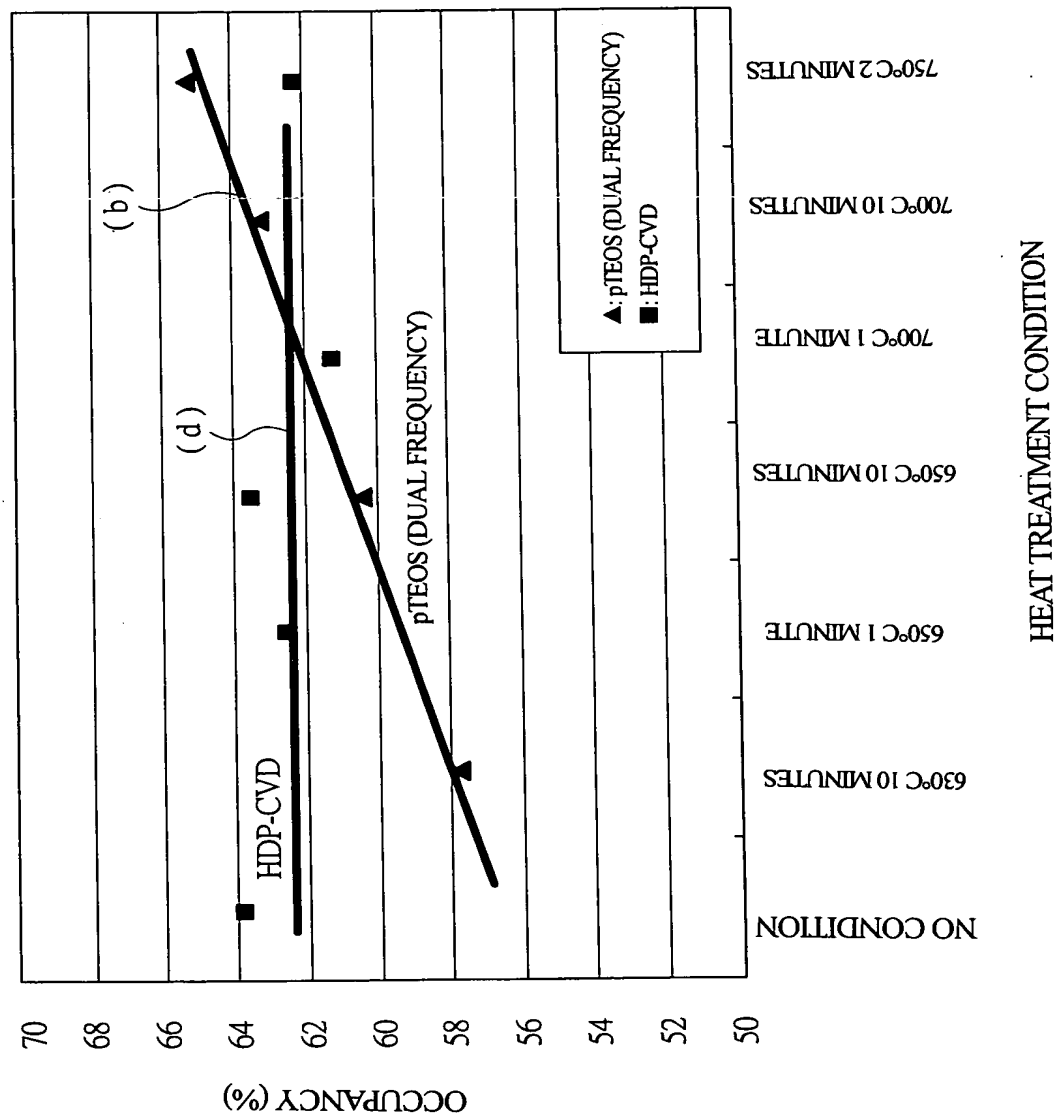


Fig. 11

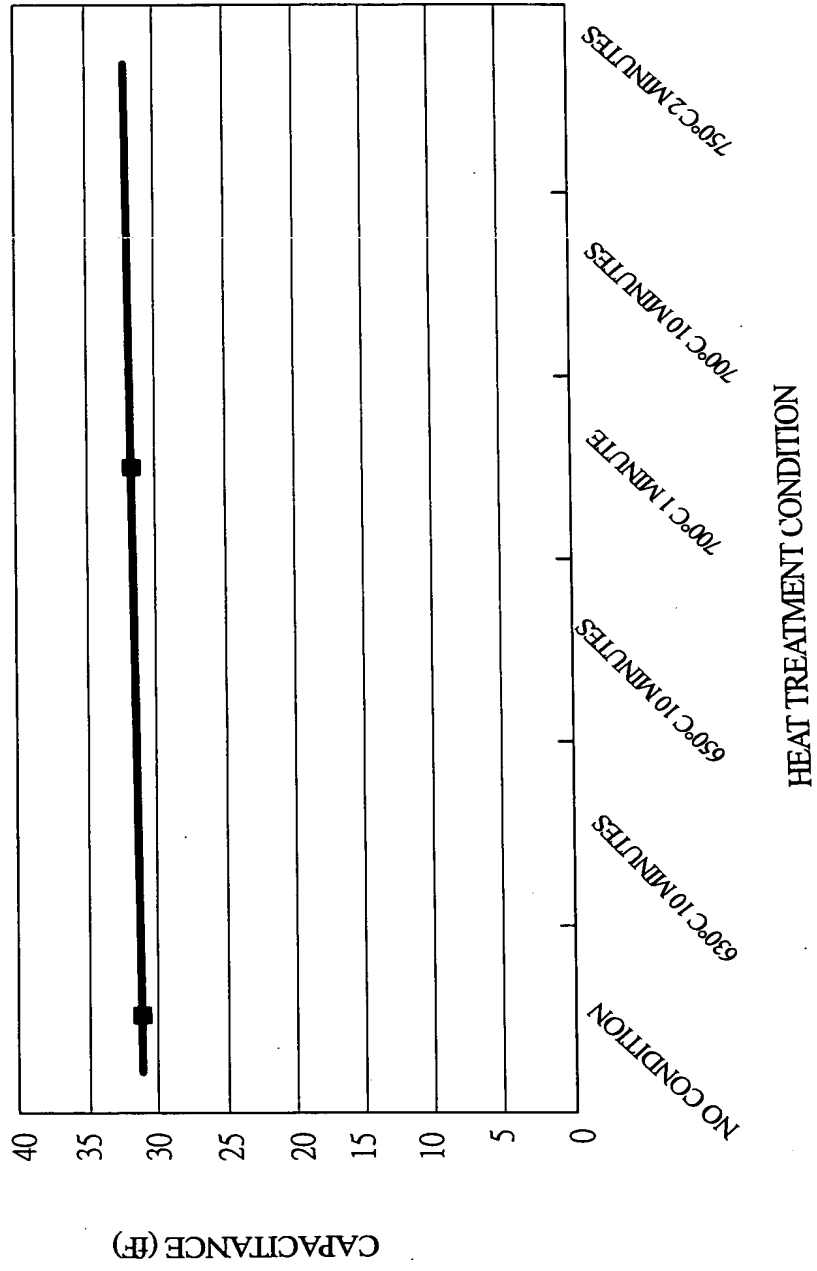


Figure 1 is a cross-sectional view of a semiconductor device, showing a memory cell forming area (MCFA) on the left and a logic circuit forming area (LCFA) on the right. The device is built on a substrate (5) with a passivation layer (6). The MCFA includes a memory cell (1) with a word line (WL) and bit line (BL) structure. The LCFA includes a logic circuit (2) with a gate stack (3) and a source/drain region (4). Various layers and structures are labeled with numbers 1 through 56.

LOGIC CIRCUIT FORMING AREA (LCFA)

Fig. 13

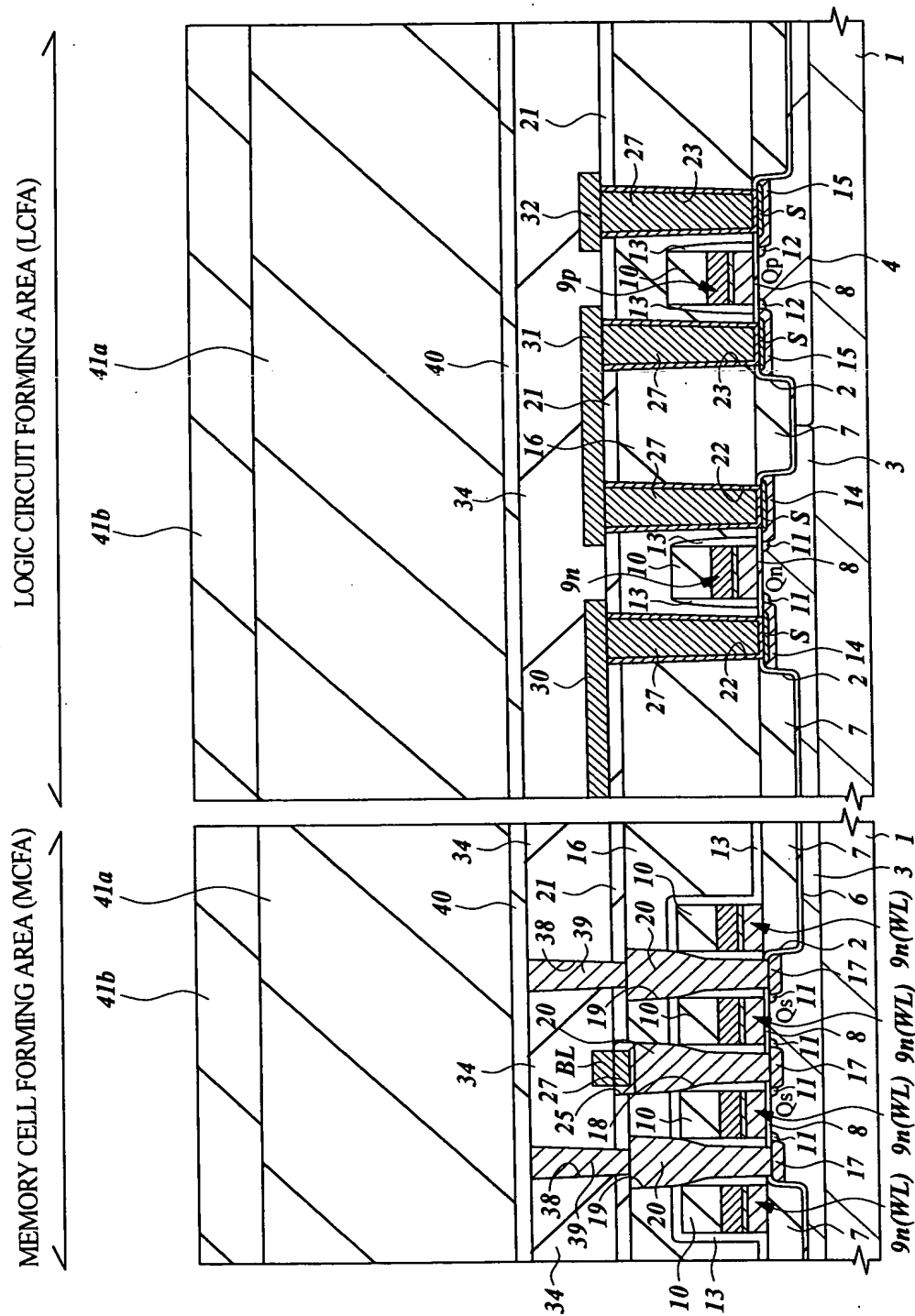


Fig. 14

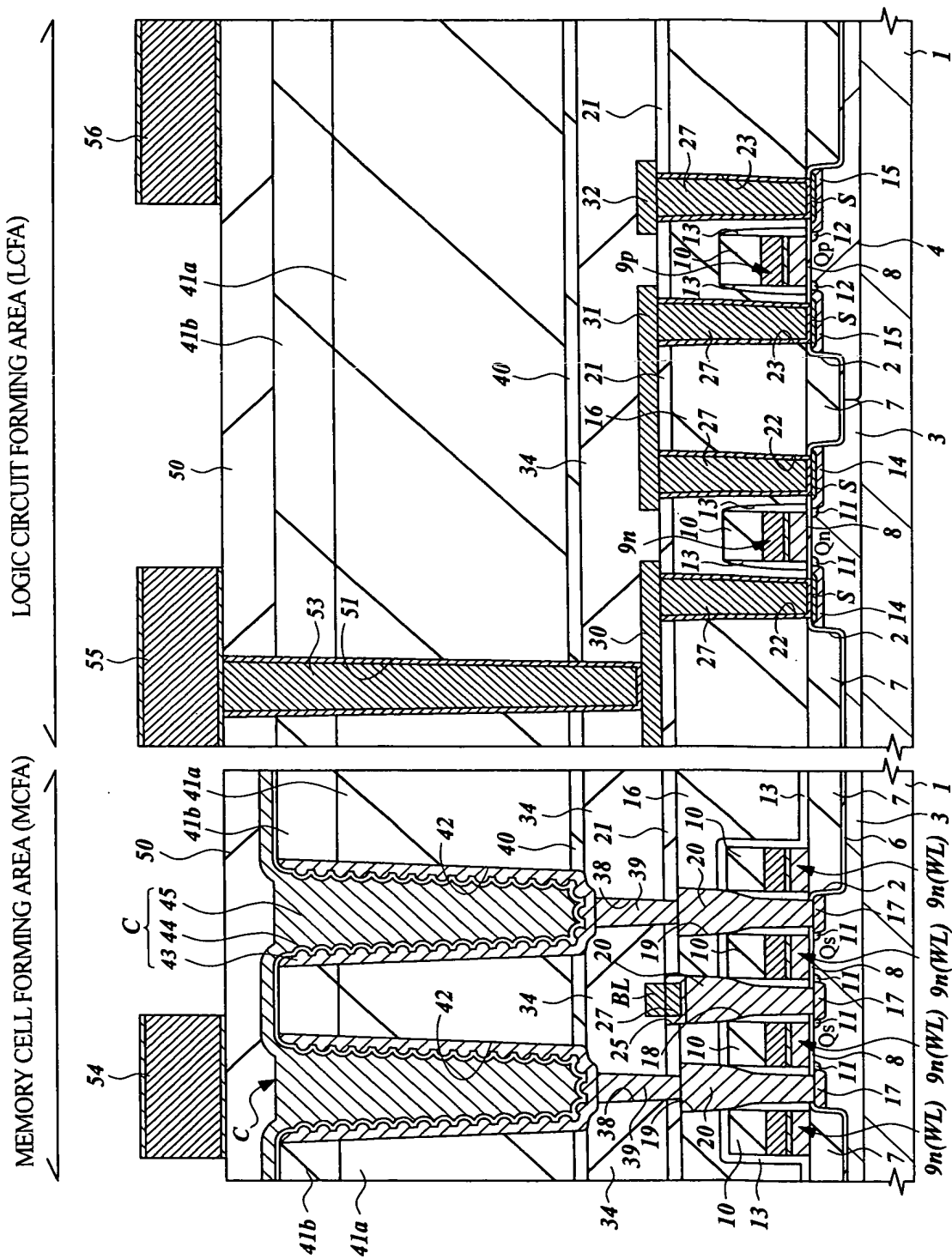


Fig. 15

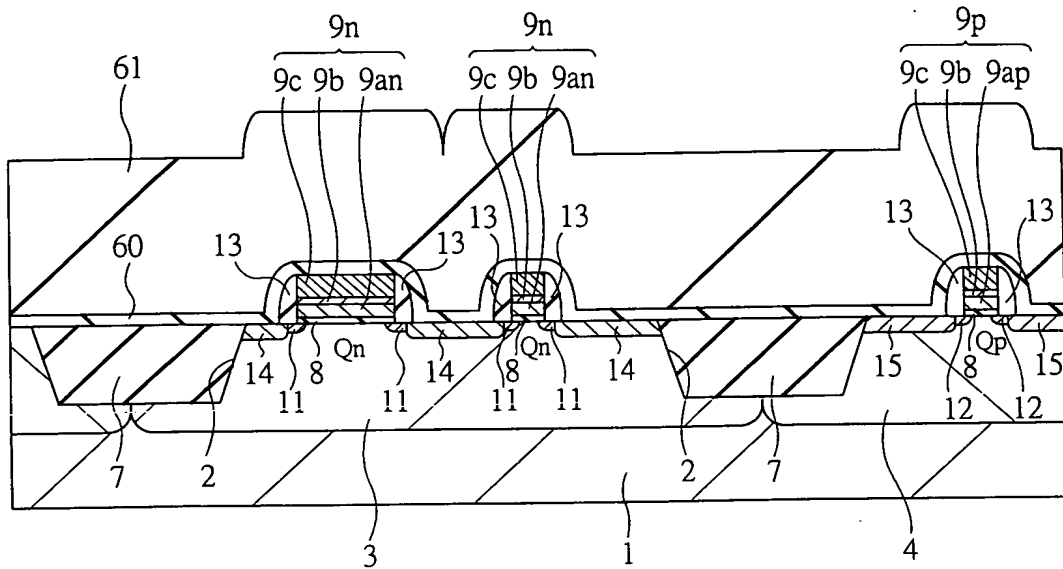


Fig. 16

